REMARKS

Claims 1-23 were examined and reported in the Office Action. Claims 1, 2, 8, 14 and 15 are rejected. Claims 1-2, 8-9, 14 and 16 are amended. Claims 1-23 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103

A. It is asserted in the Office Action that claims 1, 2, and 8 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent 6,599,821 issued to Lee ("Lee") in view of U. S. Patent 6,455,383 issued to Wu ("Wu") and U. S. Patent 5,308,655 issued to Eichman et al ("Eichman"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "[a] method for fabricating a semiconductor device, comprising the steps of: a) forming a stack layer

of a gate layer, a poly-silicon layer, a tungsten layer, and a hard mask sequentially deposited on a semiconductor substrate; b) carrying out a selective oxidation process adopting a rapid thermal process (RTP), wherein the poly-silicon layer of the stack layer is only oxidized; c) performing a heat treatment process in a low pressure chemical vapor deposition (LPCVD) furnace for releasing a stress caused by the RTP; and d) carrying out a process for forming a gate sealing nitride layer on the heat treated stack layer."

It is asserted in the Office Action that the RTP of Lee corresponds to the heat treatment process of Applicant's claimed invention, where the heat treatment process is performed in the LPCVD furnace for releasing stress. Applicant respectfully disagrees. The RTP of Lee is different from the heat treatment of the Applicant's claimed invention. The RTP of Lee is simultaneously performed with a selective oxidation process for reducing the number of the thermal processes to diminish thermal stress. (See Lee, column 4, lines 13-49). According to Applicant's claimed invention, however, the heat treatment in the LPCVD furnace is performed after the selective oxidation process (the selective oxidation process includes the RTP) to release stress caused by the RTP (see Applicant's specification, page 8, lines 22-27, to page 9, lines 1-2).

It is readily seen that Lee does not teach, disclose or suggest "b) carrying out a selective oxidation process adopting a rapid thermal process (RTP), wherein the poly-silicon layer of the stack layer is only oxidized; c) performing a heat treatment process in a low pressure chemical vapor deposition (LPCVD) furnace for releasing a stress caused by the RTP; and d) carrying out a process for forming a gate sealing nitride layer on the heat treated stack layer."

It is also asserted in the Office Action that the RTP disclosed in Wu corresponds to the heat treatment process of Applicant's claimed invention, where the heat treatment process is performed in the LPCVD furnace for releasing stress. Applicant respectfully disagrees. Distinguishable, the RTP of Wu is performed after depositing a gate sealing nitride layer by LPCVD to redistribute implanted doping impurities. Further, according to Applicant's claimed invention, after depositing a gate sealing nitride layer by LPCVD, instead of performing an RTP, the heat

treatment in the LPCVD furnace or the annealing furnace is performed to release stress generated during the selective oxidation process and the gate sealing nitride layer deposition process. Then, the RTP is performed. Therefore, Wu does not teach, disclose or suggest "b) carrying out a selective oxidation process adopting a rapid thermal process (RTP), wherein the poly-silicon layer of the stack layer is only oxidized; c) performing a heat treatment process in a low pressure chemical vapor deposition (LPCVD) furnace for releasing a stress caused by the RTP; and d) carrying out a process for forming a gate sealing nitride layer on the heat treated stack layer."

Eichman discloses a method for forming low resistivity TiN film using TiCl4 and NH3 gases by LPCVD under in-situ or under ex-situ. That is, Eichman is concerned with the point that after the TiCl4 gas flows into the LPCVD chamber, the NH3 gas flows into the LPCVD chamber for stripping off the remaining unbound chlorine within the TiN film, which may be performed in the same LPCVD chamber or in the other LPCVD chamber. Eichman, however, does not teach, disclose or suggest "b) carrying out a selective oxidation process adopting a rapid thermal process (RTP), wherein the poly-silicon layer of the stack layer is only oxidized; c) performing a heat treatment process in a low pressure chemical vapor deposition (LPCVD) furnace for releasing a stress caused by the RTP; and d) carrying out a process for forming a gate sealing nitride layer on the heat treated stack layer."

Therefore, even if Lee, Wu and Eichman were combined the resulting method will still not teach, disclose or suggest "depositing a gate sealing nitride layer on the stack layer selectively oxidized by low pressure chemical vapor deposition (LPCVD); d3) performing a heat treatment process in an LPCVD furnace or an annealing furnace for releasing a stress exerted during the selective oxidation process and gate sealing nitride layer deposition process; and e) performing a rapid thermal process (RTP) for activating source/drain regions of the semiconductor device."

Since neither Lee, Wu, Eichman nor the combination of the three teach, disclose or suggest all the limitations of Applicant's amended claim 1, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 1 is not obvious over Lee in view of Wu, and

further in view of Eichman since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 1, namely claims 2 and 8, would also not be obvious over Lee in view of Wu and further in view of Eichman for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1, 2, and 8 are respectfully requested.

B. It is asserted in the Office Action that claims 14 and 15 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Wu in view of Eichman. Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's amended claim 14 contains the limitations of "[a] method for fabricating a semiconductor device, comprising the steps of: a3) forming a stack layer of a gate oxide layer, a poly-silicon layer, a tungsten layer, and a hard mask sequentially deposited on a semiconductor substrate; b3) carrying out a selective oxidation process, wherein the poly-silicon layer of the stack layer is only oxidized; c3) depositing a gate sealing nitride layer on the stack layer selectively oxidized by low pressure chemical vapor deposition (LPCVD); d3) performing a heat treatment process in an LPCVD furnace or an annealing furnace for releasing a stress exerted during the selective oxidation process and gate sealing nitride layer deposition process; and e) performing a rapid thermal process (RTP) for activating source/drain regions of the semiconductor device."

Wu and Eichman are addressed above in section I(A) regarding Applicant's amended claim 1.

In Wu, the RTP is performed after depositing a gate sealing nitride layer by LPCVD to redistribute implanted doping impurities. Distinguishable, according to Applicant's claimed invention, after depositing a gate sealing nitride layer by LPCVD, instead of performing an RTP, the heat treatment in the LPCVD furnace or the annealing furnace is performed to release stress generated during the selective oxidation process and the gate sealing nitride layer deposition process. Then, the RTP is performed. Therefore, Wu does not teach, disclose or suggest "c3) depositing

a gate sealing nitride layer on the stack layer selectively oxidized by low pressure chemical vapor deposition (LPCVD); d3) performing a heat treatment process in an LPCVD furnace or an annealing furnace for releasing a stress exerted during the selective oxidation process and gate sealing nitride layer deposition process; and e) performing a rapid thermal process (RTP) for activating source/drain regions of the semiconductor device."

As asserted above, Eichman is concerned with the point that after the TiCl4 gas flows into the LPCVD chamber, the NH3 gas flows into the LPCVD chamber for stripping off the remaining unbound chlorine within the TiN film, which may be performed in the same LPCVD chamber or in the other LPCVD chamber. Eichman, however, does not teach, disclose or suggest "c3) depositing a gate sealing nitride layer on the stack layer selectively oxidized by low pressure chemical vapor deposition (LPCVD); d3) performing a heat treatment process in an LPCVD furnace or an annealing furnace for releasing a stress exerted during the selective oxidation process and gate sealing nitride layer deposition process; and e) performing a rapid thermal process (RTP) for activating source/drain regions of the semiconductor device."

Therefore, even if Wu and Eichman were combined the resulting method will still not teach, disclose or suggest "c3) depositing a gate sealing nitride layer on the stack layer selectively oxidized by low pressure chemical vapor deposition (LPCVD); d3) performing a heat treatment process in an LPCVD furnace or an annealing furnace for releasing a stress exerted during the selective oxidation process and gate sealing nitride layer deposition process; and e) performing a rapid thermal process (RTP) for activating source/drain regions of the semiconductor device."

Since neither Wu, Eichman nor the combination of the two teach, disclose or suggest all the limitations of Applicant's amended claim 14, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 14 is not obvious over Wu in view of Eichman since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that directly depends from amended claim 14, namely claim 15, would also

not be obvious over Wu in view of Eichman for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 14 and 15 are respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 3-7, 9-13 and 16-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-23, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-23 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: April 25, 2005

By: _____
Steven Laut, Reg. No. 47,736

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop A/F, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on April 25, 2005.

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Jean Svoboda